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A NEW APPROACH TO FRONT END INTERFACE DC-DC CONVERTER

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Abstract:

This paper presents a new zero voltage-switching (ZVS) isolated front end interface dc–dc converter which combines a boost half bridge (BHB) cell and a full-bridge (FB) cell, so that two different type of power sources, i.e., both current fed and voltage fed, can be combined togetherly by the proposed soft switched converter for various applications, such as fuel cell and hybrid systems. By using two high-frequency transformers and a combined leg of switches, number of switches and gate driver circuits can be minimized. By phase-shift control, the converter can achieve ZVS turn-on of active switches and zero-current switching (ZCS) turn-off of diodes. In this paper, derivation, analysis, and design of the proposed converter are presented. Finally, a 5–10V input, 600–700Voutput prototype with a 600W nominal power rating is built up and tested to demonstrate the effectiveness of the proposed converter topology.

1. Introduction:

Nowadays, clean and renewable energies including fuel cell, wind energy, photovoltaic, etc., have been widely applied to achieve environment friendly objectives because of the discontinuity of renewable sources, like wind energy and solar energy, generally, an auxiliary power supply is necessary to smooth output power and keep output voltage stable under various load conditions. Due to the unregulated dc output voltage, the low dynamics, and the discontinuity of renewable energy sources, like solar energy and fuel cell, generally, it is well known that not only a front-end dc–dc converter as an interface circuit is required, but also an auxiliary power supply is needed to compensate or regulate output power seamlessly at different load conditions.

Therefore, an efficient hybrid renewable power conversion system has become an interesting topic. In terms of the applications with a galvanic isolation, various system configurations have been investigated in the last decade, and usually they can be divided into three categories, i.e., direct hybridization, multiple-stage conversion and multiple-port conversion. The main disadvantage of this system is that if one input source is connected, only one converter will be operated and the other one will be completely under the idle condition that will reduce the power density of the whole system. Due to this reason, multi-port converters have been proposed and received more and more attention in recent years. With different specifications and requirements, the adequate converter and/or configuration can be adopted.

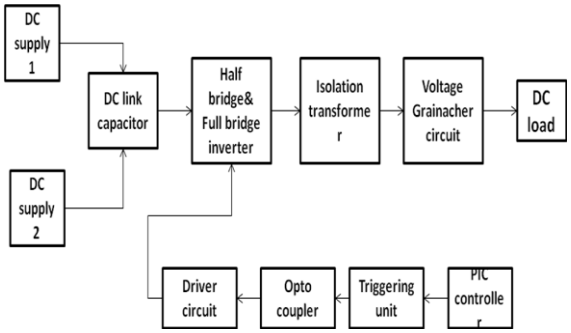

Figure (1): Block diagram of a of a dual-input converter with BHB and FB cells

The salient advantages of the proposed converter can be summarized as follows:
1) Ability of dual-input connection;
2) Reduced number of power devices and their associated gate driver components;
3) ZVS turn-on of the main switches;
4) ZCS turn-of of the diode switch out reverse recovery issue.

2. Proposed Soft-Switched DC–DC Converter:

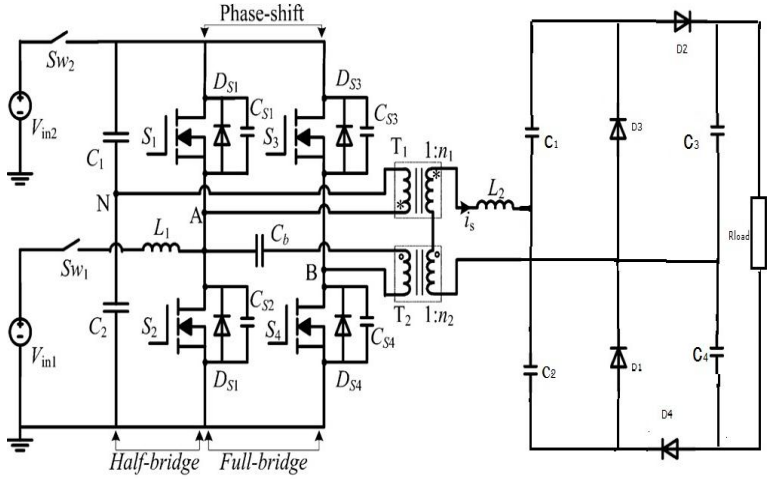

Figure (2): Proposed hybrid DC–DC converter

Mode 1:

During [t_0 ,t_2], as shown in Figure 3.3, the body diodes of S1 and S4 conduct and V_p is clamped to a voltage of $2V_L$ until is decreases with a slope $(2V_L + V_H)/L_2$ to zero at t_2 .At t_0 ,S1 turns ON under ZVS

Mode 2:

During [t_2, t_3], when I_s becomes positive and flows through D1, S1 and S4 will conduct and is increases with a slope $(2V_L - V_H)/L_2$.

Mode 3:

During [t3, t5], when S4 turns OFF at t3, CS3 and CS4 start to resonate with L2 until VCS3 = 0, and then S3 can turn ON under ZVS. Current in the primary side flows through S1 and DS3 that makes V_p equal to VL, and is decreases with a slope (V − V)/L.
A voltage doubler circuit is employed on the secondary side and the voltage ringing over the diodes can inherently be clamped by the output capacitor C3 or C4 . L2 is essentially the sum of the transformer leakage inductance and an extra inductance. A dc blocking capacitor Cb is added in series with the primary winding of T2 in order to avoid transformer saturation caused by any asymmetrical operation in the FB circuit.

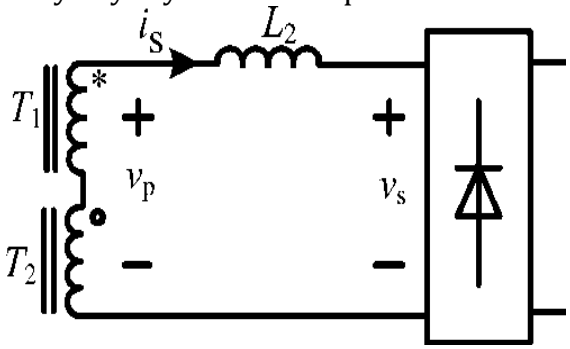

Figure (3): Equivalent circuit of phase-shift control.

Same as the dual active bridge (DAB) converters, the pro- posed converter can be viewed as a voltage source vp interfaced to another voltage source vs through the

energy interfacing element L2 as shown in Fig. 3. In steady state, the timing diagram and the key waveforms of the proposed converter controlled by phase-shift angle between the s witch pairs, S1 , S2 and S3 , S4 .

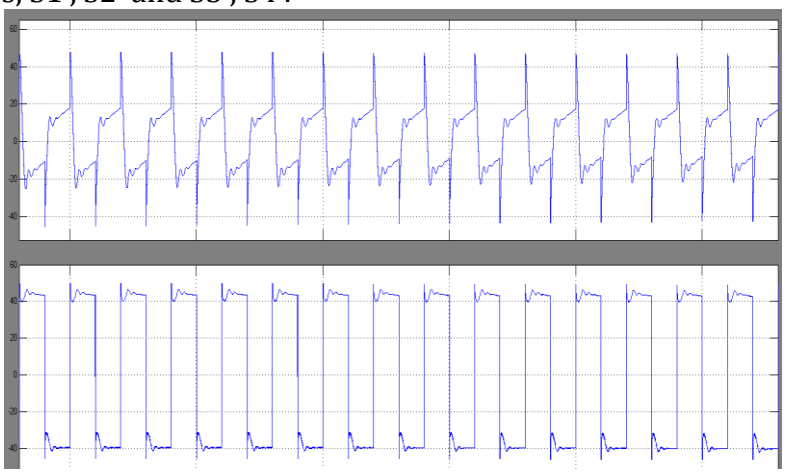

Figure (4): Output of BHB and FB Circuit

In this paper, only the symmetrical operation condition, i.e., the switching duty cycle D is 50%, is discussed, so that S1 and S2 as well as S3 and S4 have the complementary driving signals that gives Vin2 = 2Vin1 . Accordingly output voltage and power transferred can only be regulated by the phase-shift angle α of the two poles of the input bridge. The power factor of the high frequency ac loop can be evaluated by the angle ϕ which represents the phase delay between the secondary voltage and current. In order to avoid high reactive power in the converter, the regulated phase-shift angle will be limited in the range: $0 \le \alpha \le \pi$, in the practical applications.

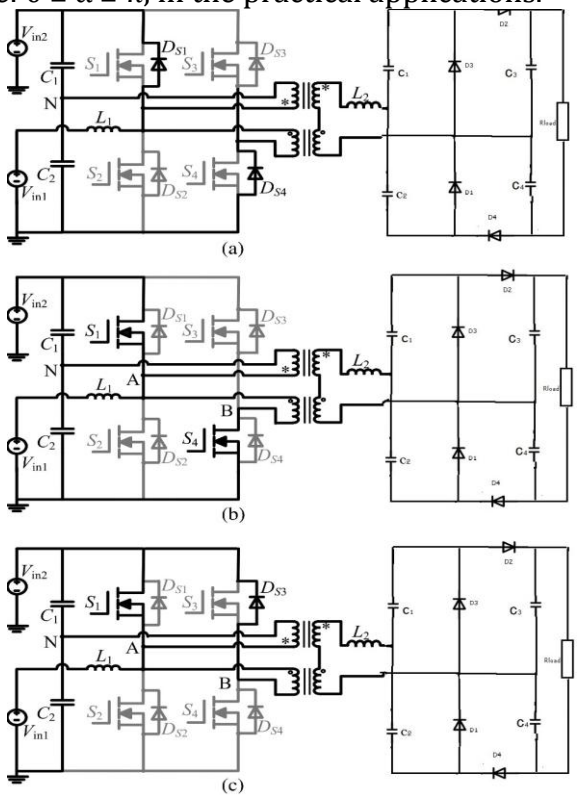

Figure (5) Equivalent circuits of the proposed converter: (a) [t0 , t2], (b) [t2 , t3] and (c) [t3 , t5].

Since the output diode rectifier is current driven, the following constrains must be satisfied: 1) when I_s is positive, vs must be positive; and 2) when I_s is negative, vs must be negative, and thereby based on the waveforms shown in the Fig. 4(a), the operation principle of the converter can be explained as follows. During [t0 , t2], as shown in Fig. 5(a), the body diodes of S1 and S4 conduct and Vp is clamped to a voltage of 2VL until is decreases with a slope (2VL + VH)/L2 to zero at t2 . At t0 , S1 turns ON under ZVS. During [t2 , t3], when is becomes positive and flows through D1 , S1 and S4 will conduct and is increases with a slope (2VL − VH)/L2 , as shown in Fig. 5(b). During [t3 , t5], when S4 turns OFF at t3 , CS 3 and CS 4 start to resonate with L2 until VC S 3 = 0, and then S3 can turn ON under ZVS. Current in the primary side flows through S1 and DS 3 that makes vp equal to VL , and is decreases with a slope
(VH − VL)/L2 . The equivalent circuit is given in Fig. 5(c).
After t5 the second half switching cycle starts. Obviously, the diodes on the secondary side will always turn OFF under ZCS in the whole operation range
From the typical waveforms in fig 4(a) the defined peak current values I_1 and I_2 are given as

$$I_1 = i_s(t3) = \frac{2VL - VH}{L2} \cdot \frac{(\propto -\varphi)T_s}{2\pi} \qquad (1)$$

$$I_2 = i_s(t5) = \frac{2VL + VH}{L2} \cdot \frac{(\varphi)T_s}{2\pi} \qquad (2)$$

$$I1 - I2 = \frac{VH - VL}{L2} \cdot \frac{(\pi - \propto)T_s}{2\pi} \qquad (3)$$

To determine the value of phase delay we can solve (3) for ϕ rad.

$$\Phi = 1/4(\pi + \alpha - V_H/V_L\,\pi) \qquad (4)$$

Substituting (4) into (1) and (2), the output power of the pro- posed converter can be expressed

$$P_o = f(\alpha) = \begin{cases} \frac{V_H V_L}{4\omega L_2}\left(1 - \frac{V_H^2}{V_L^2}\right), & 0 \le \alpha \le \varphi \\ \frac{V_H V_L \pi\left[-3\left(\frac{\alpha}{\pi}\right)^2 + 6\left(\frac{\alpha}{\pi}\right) + \left(1 - \frac{V_H^2}{V_L^2}\right)\right]}{8\omega L_2}, & \varphi < \alpha \le \pi \end{cases}$$

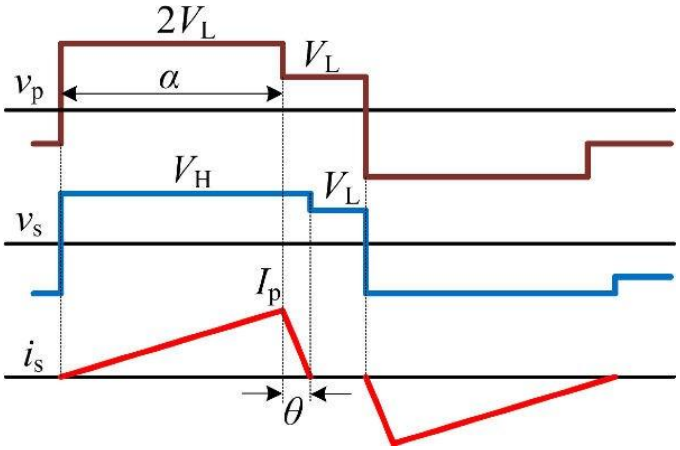

Figure (6):Typical waveforms under discontinuous I_s

Hence, the constraints to keep is in continuous conduction mode can be yielded

3. Design Considerations:

Generally, ZVS can be deduced on the precondition that the anti parallel diode of switch must conduct before the switch is triggered. In other words, the main devices are turned OFF with a positive current flowing and then the current diverts to the opposite diode which allows the in-coming MOSFET to be switched on under zero voltage. There for ZVS constraints depend on the magnitude of primary side currents ie.,(n1+n2).is,IL1 and n2 .is and have the relationships at driving instant.

$-(n1+n2).i_s(t1)-iL1(t1)<0$, for S1
$(n1+n2).i_s(t5)-iL1(t5)>0$ for S2
$(n2).i_s(t3)>0$ for s3,s4

The voltage gain versus phase-shift angle α is plotted in Fig. 6 under the conditions: Vin1 = 25 V, Vin2 = 2•Vin1 = 50 V, L2 = 40 μH, n1 = 4, n2 = 2, load resistance R = 300 Ω, and switching frequency fs = 100 kHz. It is clear that the results from calculation and simulation (MATLAB/PLECS is adopted

If we assume the switching frequency is constant, apparently (10) may not be satisfied when a larger input filter inductance L1 is employed, and furthermore the ZVS range as a function of α and L2 with different loads can be illustrated in Fig. 8. It can be found that increasing L2 and/or decreasing R can enlarge the ZVS region at the cost of the reduced power delivering capability.

For converters with low input voltage and high current, turn- off loss of the switches on the low voltage side is the predominating factor of the switching loss [2], which cannot be ignored and is closely related to the stress of switch-off current. More-over, during converter design, it is also necessary to compute the root mean square (rms) values of the switch current to estimate conduction loss as for choosing MOSFETs, especially for the power devices located in the high current path. As an example, when input voltage is 30 V, Fig. 9 plots the values of transient turn-off current and rms current of the devices on the primary side as a function of α. It can be seen that the current stress is not distributed equally and among the switches, S2 will have to handle highest current stress and also high conduction loss owing to the BHB structure. Both the turn-off transient cur- rent and the rms current of S2 are approximately proportional to the phase-shift angle that means for same output power, if α decreases, switching and conduction losses of S2 will become less, so as a result the system efficiency can be improved. Regarding to this fact as well as the ZVS operation, an optimal design and tradeoff between switching loss and conduction loss may be considered for the future research.

TABLE I
PARAMETERS AND COMPONENTS USED IN HARDWARE

Parameters	*Values*
Input voltage	25-50 VDC
Rated output power	600 W
S_1 and S_2	SUP90N15 (150 V/90 A)
S_3 and S_4	SUP28N15 (150 V/28 A)
D_1 and D_2	15ETL06FP (600 V/15 A)
Transformers T_1 and T_2	4:16, 8:16, Ferrite N87
Inductors L_1 and L_2	20μH, KoolMμ; 40μH, N87
Switching frequency	100 *k*Hz

When α = 0.2π, the experimental waveforms of voltage vp and vs , and input filter current iL 1 and secondary side ac current is are presented from top to bottom in Fig. 10(a). The voltage and current waveforms in the cases where α = 1.6π and is conducts discontinuously (α = 0.2π, L2 = 20 μH) are shown in Fig. 10(b) and (c), respectively. The waveforms of gate-source voltage vG S and drain-source voltage V_D S of S2 and S4 with ZVS turn-on operation are given in Fig. 11. Based on the measurement from the prototype, the measured output voltage versus α at input voltage of 25 V is plotted in Fig. 12 in order to verify the effectiveness of the theoretical analysis. Finally, the efficiency curve at input voltage of 30 V and output voltage of 380 V is plotted in Fig. 13, and the maximum efficiency can reach 98% at 250 W.

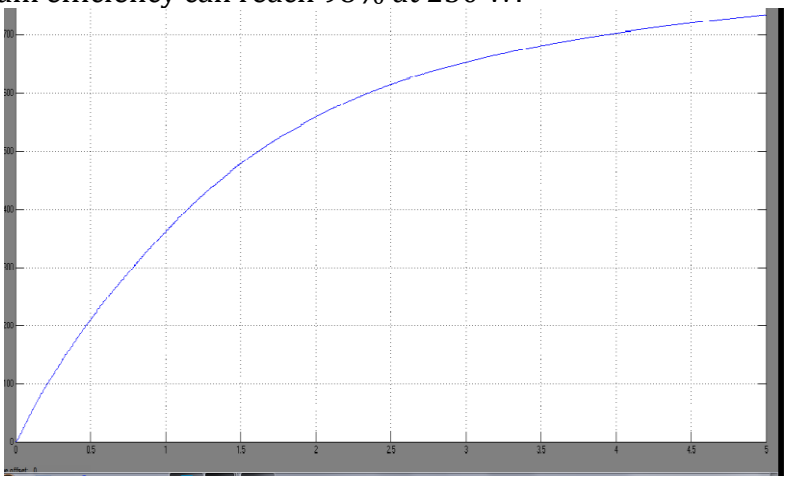

Figure (7): Output of the proposed converter

4. Conclusion:

In this proposed paper, a soft-switched isolated dc–dc converter with the ability of handling two independent inputs is derived, investigated, and designed. Comparing to the existing topologies, the converter proposed here has the advantages such as reduced number of power switches, higher efficiency, and simple control. While, the main drawback is unequally distribution of current Stress among the power devices so that it will increase the design complexity.

In the future research, some issues or topics such as asymmetrical control, dual-input operation and control, and dead-time effect, an optimal design and tradeoff between switching loss and conduction loss may be considered.

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