



SPWM BASED NINE LEVEL DIODE CLAMPED MULTILEVEL INVERTER FOR INDUCTION MOTOR DRIVE

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Abstract:

In this paper, elimination harmonics in a nine level diode-clamped multilevel inverter (DCMLI) has been implemented by using fundamental modulation switching. The Hybrid Selective Harmonic Elimination SPWM based nine level diode climbed multilevel Inverters to eliminates harmonics by generating negative harmonics with switching angles calculated for selective harmonic elimination method. In this paper an easy to implement procedure is proposed for generating PWM firing signals for higher level DCMLI This method used for single source only .In order to confirm the proposed method, first MATLAB simulation results are given.

1. Introduction:

In recent years multilevel inverters have become a very interesting field of study in what regards their industrial application. These converters allow the synthesizing of a sinusoidal voltage waveform starting from several levels of dc voltages. However, besides that advantage there are other important advantages such as, reduced switching losses, low dv/dt 's and reduced common mode voltages. Due to these characteristics several multilevel inverter topologies have been developed.

The diode-clamped multilevel converter is one of the most used multilevel topologies. This power converter consists of two capacitor voltages in series and uses the central tap as the neutral .However; this power converter needs a complex control system in order to balance the capacitor voltages. The flying capacitor converter is another of the important multilevel topologies. This multilevel structure does not need clamping diodes, but still has dc-link voltage unbalancing problems. The third important multilevel topology is the cascade H-bridge inverter.

This last multilevel inverter has become very important due to its modular structure and easiness of operation. Another advantage is that does not have the voltage balancing problems common to dc capacitors of diode-clamped or flying multilevel inverter. However, this topology has an important disadvantage related with the required number of isolated dc sources. In order to maximize the number of the inverter output voltage levels, the amplitude of all DC sources devoted to supply the H-bridge cells must obey a certain relation.

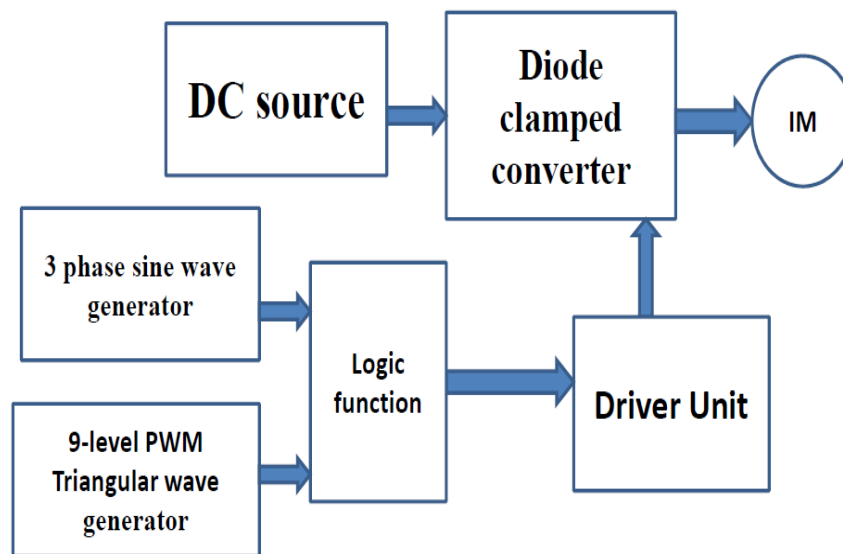


Figure (1): Block Diagram

A multilevel power converter with the structure of the cascade H-bridge inverter but using only one DC source was also proposed. This topology uses an H-bridge with a dc source and another H-bridge where the dc voltage source is only a capacitor. Multilevel inverters have also applied to induction motors with open-end windings. In this paper instead of a classical multilevel inverter; it is proposed a hybrid multilevel inverter with a single dc source to drive open-end induction motors. The proposed topology includes a three-phase H-bridge inverter supplied by a dc voltage and three single-phase H-bridge inverters with a capacitor as DC voltage supply. To maximize the output voltage levels of the hybrid multilevel inverter, the voltage of the single-phase inverters is half of the value of the three phase bridge inverter DC source. To control this multilevel structure two control loops are used. For the three-phase H-bridge inverter a SPWM modulator controlled by a proportional-integral (PI) controller is used to enforce the d component of the three-phase currents. For the single-phase H-bridge inverters a sliding mode controller (to maintain the capacitor voltage near the required value) and a simple integral controller for the q component of the three-phase currents are used.

2. Diode Clamped Multilevel Topology Using A Single DC Source:

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The circuit for a diode clamped inverter for a three-level and a four-level inverter. The key difference between the two-level inverter and the three-level inverter are the diodes D1a and D2a. These two devices clamp the switch voltage to half the level of the dc-bus voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is $V_{dc} / n-1$. Although each active switching device is only required to block $V_{dc} / n-1$, the clamping devices have different ratings. The diode clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level.

The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced..

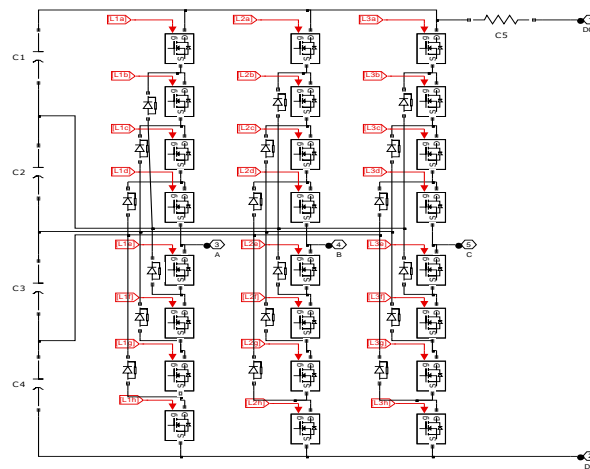


Figure (2): Power circuit

Symmetrical dual three-phase system with common-mode voltage elimination is based on two standard three-phase inverters, with the 600-phase-shift of signals of the two inverters. Basic schemes of synchronized PWM, applied for control of both two-level and three-level inverters, have been analyzed and compared.

However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been limited to the three levels. Because of industrial developments over the past several years, the three level inverter is now used extensively in industry applications. Although most applications are medium-voltage, a three-level inverter for 480V is on the market. Extending the diode-clamped concept to four levels results in the topology. A pair of diodes is added in each phase for each of the two junctions. The operation is similar to the three-level. For practical implementation, the switching state needs to be converted into transistor signals. Once the transistor signals are established, general expressions for the a-phase line-to-ground voltage and the a-phase component of the dc currents can be written as

$$V_{ao} = H_{aN}V_{N0} + H_{aN-1}V_{N-10} + \dots + H_{a1}V_{10}$$

$$V_{bo} = H_{bN}V_{N0} + H_{bN-1}V_{N-10} + \dots + H_{b1}V_{10}$$

$$V_{co} = H_{cN}V_{N0} + H_{cN-1}V_{N-10} + \dots + H_{c1}V_{10}$$

The node currents for the N level inverter are given by

$$I_N = H_{aN}I_a + H_{bN}I_b + H_{cN}I_c$$

$$I_{N-1} = H_{aN-1}I_a + H_{bN-1}I_b + H_{cN-1}I_c$$

$$I_1 = H_{a1}I_a + H_{b1}I_b + H_{c1}I_c$$

The above relationships may be programmed into simulation software to form a block that simulates one phase of a diode-clamped inverter. A number of blocks can be connected together for a multiphase system. For more simulation details, the transistor and diode KVL and KCL equations may be implemented. This allows inclusion of the device voltage drops (as well as conduction losses) and also the individual device voltages and currents. To express this relationship, consider the general N-level diode-clamped structure. Therein, only the upper half of the inverter is considered since the lower half contains complementary transistors and may be analyzed in a similar way. Through the clamping action of the diodes, the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank.

The inner diodes of the multilevel inverter must block a higher voltage. For example, in the four-level topology the inner diodes must block two-thirds of the dc voltage while the outer diodes block one-third. This is a well-known disadvantage of the diode-clamped topology. For this reason, some authors represent the higher voltage diodes with lower voltage diodes in series or alter the structure of the topology so that each diode blocks the same voltage. Finally, the capacitor junction currents may be expressed as the difference of two clamping diode currents. In case of a three-level inverter, the expression.

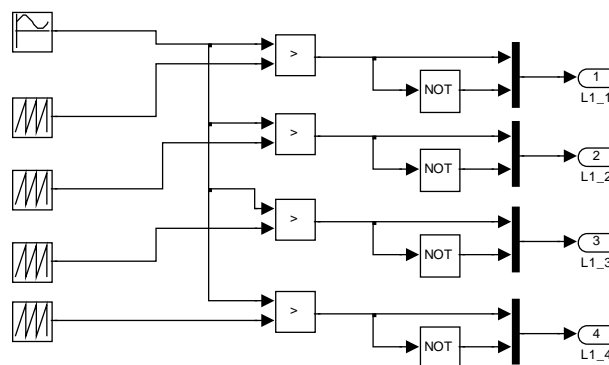


Figure (3): Control Circuit

An m -level diode-clamped multilevel inverter typically consists of $m - 1$ capacitors on the dc bus and produces m levels of the phase voltage. A three-phase five-level structure of a DCMLI. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into five levels. The voltage across

each capacitor is V_{dc} , and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes.

Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg a are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, and $(S_{a4}, S_{a'4})$. Table 1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series. To evaluate the dynamic performances of the proposed hybrid cascaded multilevel inverter and the control system, numerical simulations have been carried-out. The parameters of the simulated system are presented.

Voltage V_a	SWITCH STATE							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_4 = 4V_{dc}$	1	1	1	1	0	0	0	0
$V_3 = 3V_{dc}$	0	1	1	1	1	0	0	0
$V_2 = 2V_{dc}$	0	0	1	1	1	1	0	0
$V_1 = V_{dc}$	0	0	0	1	1	1	1	0
$V_0 = 0$	0	0	0	0	1	1	1	1

Figure (4): DCMLI Voltage Levels and Switching States

3. Simulation:

The output voltage of the proposed multilevel inverter is presented. As can be seen in this Figure the output voltage has seven levels. This is achieved due to the relation between the amplitude of the DC voltage source and the capacitors voltage. The DC voltage of the capacitors is regulated to half the value of the DC source voltage. It shows the three-phase output currents waveforms. From this result it is possible to verify that the multilevel inverter provides near sinusoidal currents. The capacitor voltage is plotted in Fig. 7 as a function of time. This result shows that the capacitor voltage is maintained closed to the set point. Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off.

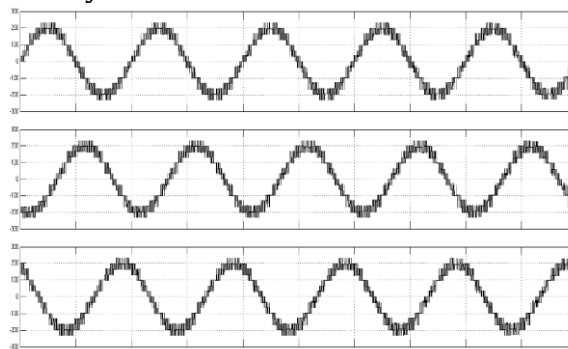


Figure (5): Result of the Output Voltage Waveform

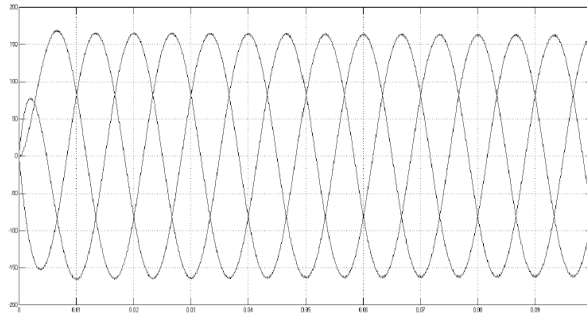


Figure (6): Result of the Load Voltage Waveform

Since nearly all multilevel inverters involve effective series connection of transistor devices, parallel connection of inverter poles through inter-phase reactors is sometimes overlooked or not recognized as a multilevel solution. However, researchers noted the features and redundancies of multilevel some time ago. One advantage of parallel connection is that the devices share current and this topology is good for high current loads. It is also reasonable to perform parallel combinations of diode-clamped poles so that the transistor voltage and current ratings are reduced. The inverter consists of familiar H-bridge (sometimes referred to as full-bridge) cells in a cascade connection. Since each cell can provide three voltage levels (zero, positive dc voltage, and negative dc voltage), the cells are themselves multilevel inverters. Since the H-bridge cells can supply both positive and negative voltages contributing to the line-to-ground voltage, a switching state is defined for H-bridge cells that have negative values. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. An apparent disadvantage of this topology is the large number of isolated voltages required to supply each cell. However, phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

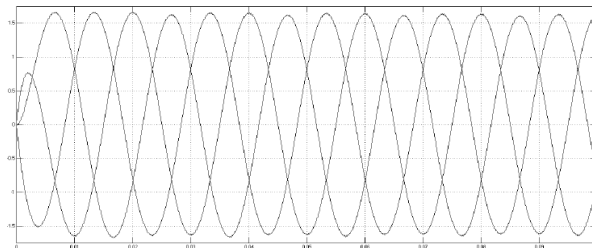


Figure (7): Result of the Load Current Waveform

4. Conclusion:

The diode clamped and Cascaded 3-phase nine level multilevel inverter is simulated for sinusoidal PWM technique and modified space vector PWM technique. The simulation results with harmonic spectrum are presented in this paper. To evaluate the dynamic performances of the proposed hybrid cascaded multilevel inverter and the control system, numerical simulations have been carried-out. It is concluded that modified reference SVPWM technique has given good harmonic spectrum with fundamental and THD when compared with other techniques for Cascaded five level inverter. Total harmonics reduction purpose used for dq transformation PWM scheme Converter switching losses reduction purpose used for new control scheme based soft switching. Experimental results show that the proposed hybrid SHEPWM scheme could meet the modulation index need of the motor and reduce the common mode voltage in the drive, and the two SHEPWM schemes could transition smoothly.

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